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NON-LINEAR DISTRIBUTION OF VOLTAGE STEPS IN FLASH-TYPE A/D CONVERTERS

• This application is a 371 of PCT/1003/05507 Filed on 11/28/2003
which claims benefit of 601430, 920 12-4-02,

The present invention relates to a method, apparatus, and system for converting an input

5 voltage to a digital output.

Current flash-type analog-to-digital (A/D) converters are characterized by high relative error at low input voltage. Accordingly, there is a need for a method, apparatus, and system that efficiently reduces the relative error in the digital output of a flash-type A/D converter at low input voltage.

10 In first embodiments, the present invention provides a flash-type analog-to-digital (A/D) converter, said A/D converter adapted to convert an input voltage VIN to a digital output, wherein VIN is within a working voltage range of the A/D converter, said working voltage range defined by a lowest voltage VREF- and a highest voltage VREF+, said A/D converter comprising:

15 N reference voltages V1, V2, ..., VN non-linearly distributed between VREF- and VREF+ and ordered according to $VREF- < V1 < V2 < \dots < VN < VREF+$, wherein N is at least 3;
N comparators associated with said N reference voltages on a one-to-one basis, each comparator adapted to make a comparison between VIN and the reference voltage that is associated with said comparator, each comparator adapted to generate a binary bit that
20 reflects a binary result of said comparison; and
encoder means for generating the digital output from an analysis of the binary bits generated by said comparators.

In second embodiments, the present invention provides a method for converting an input voltage VIN to a digital output such that VIN falls between a lowest voltage VREF- to a
25 maximum voltage VREF+, said method comprising:
providing N reference voltages V1, V2, ..., VN non-linearly distributed between VREF- and VREF+ and ordered according to $VREF- < V1 < V2 < \dots < VN < VREF+$, wherein N is at least 3;;
comparing VIN with each of the N reference voltages;
30 generating a binary bit for each said comparisons, said binary bit reflecting a binary result of said comparison; and
generating the digital output from an analysis of the generated binary bits.